IN2P3

Omega

LAL

ADC Measurements
PARISROC Chip

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OMEGA / LAL Orsay

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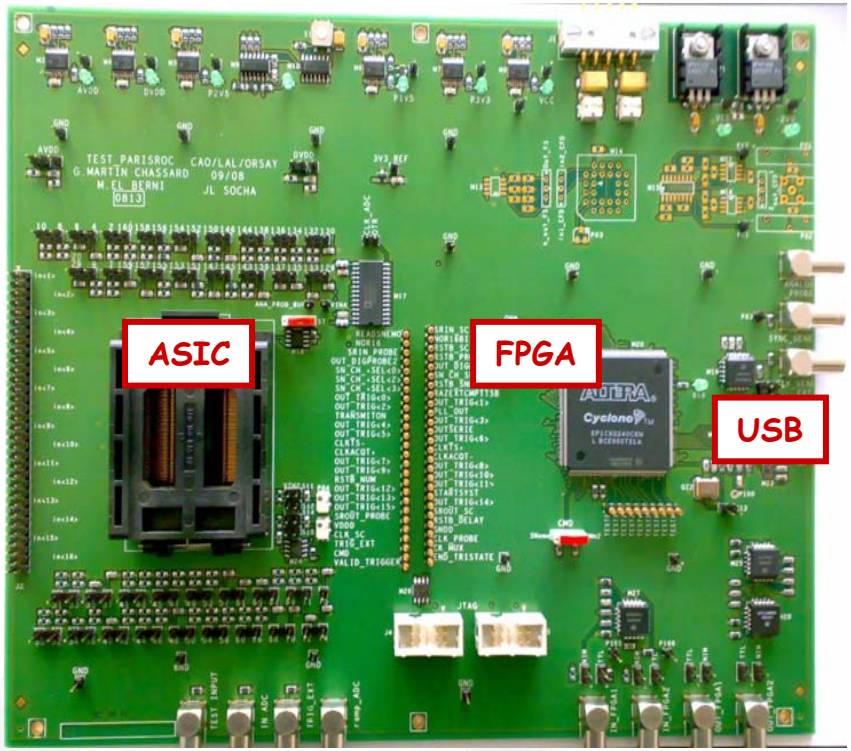
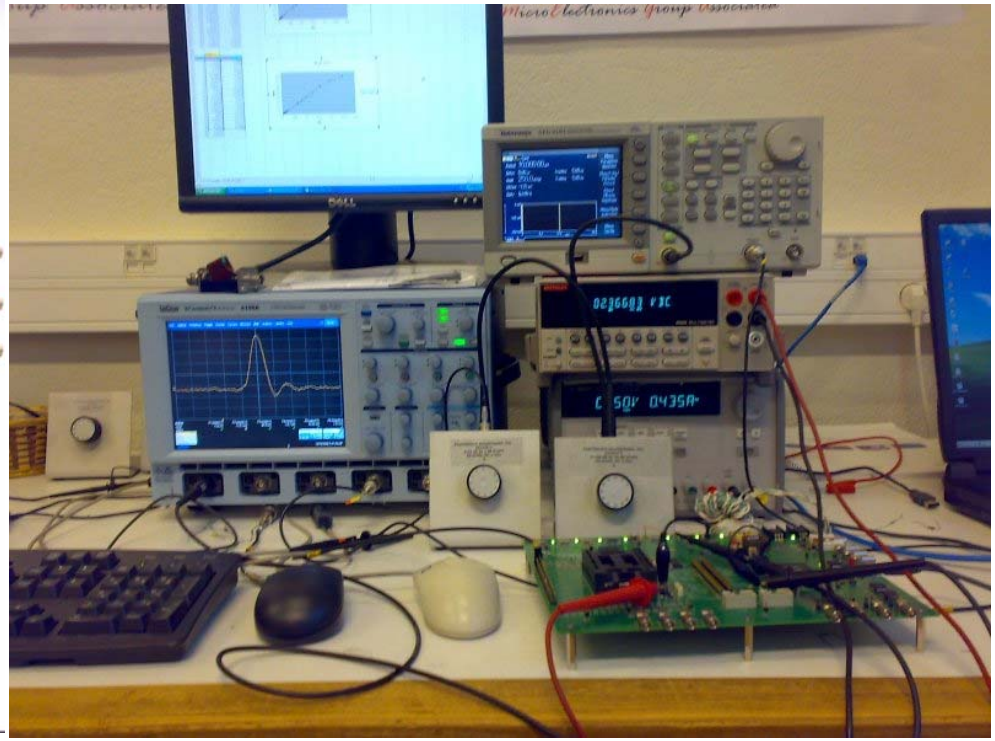
PARISROC ADC Measurements

TEST BOARD



TEST BENCH

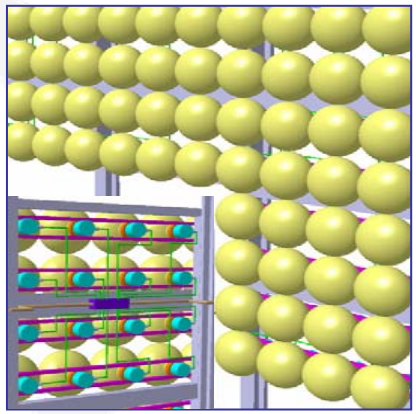


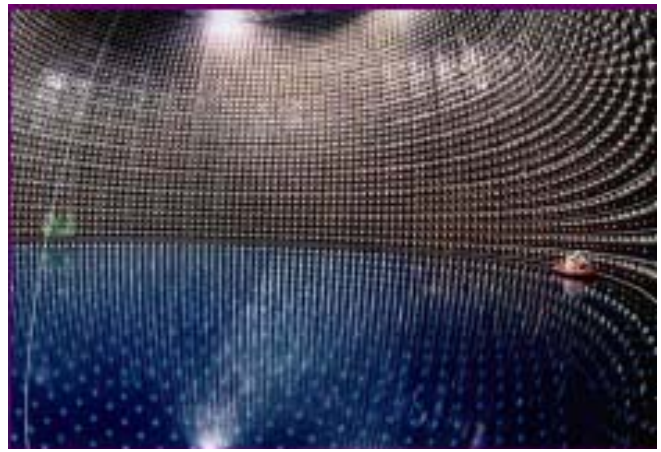
PMm² Project

- ***PMm² :*** ***"Innovative electronics for array of photodetectors used in High Energy Physics and Astroparticles".***

- **R&D program funded by French national agency for research (ref. ANR-06-BLAN-0186) (LAL, IPNO, LAPP , ULB Bruxells and Photonis) (2007-2010)**

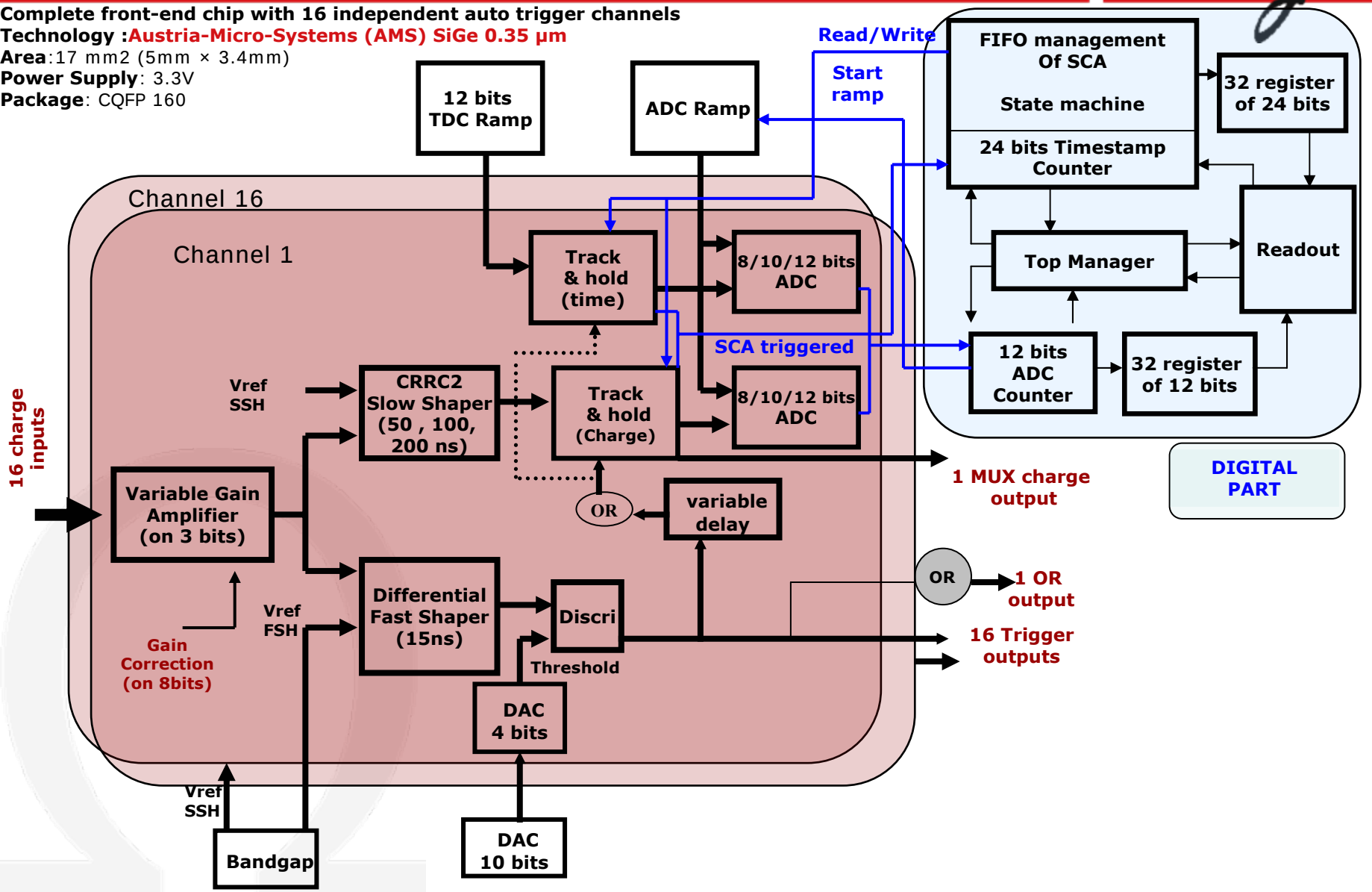
- **Application : large water Cerenkov neutrino detectors (more generally: exp. with large number of PMTs)**



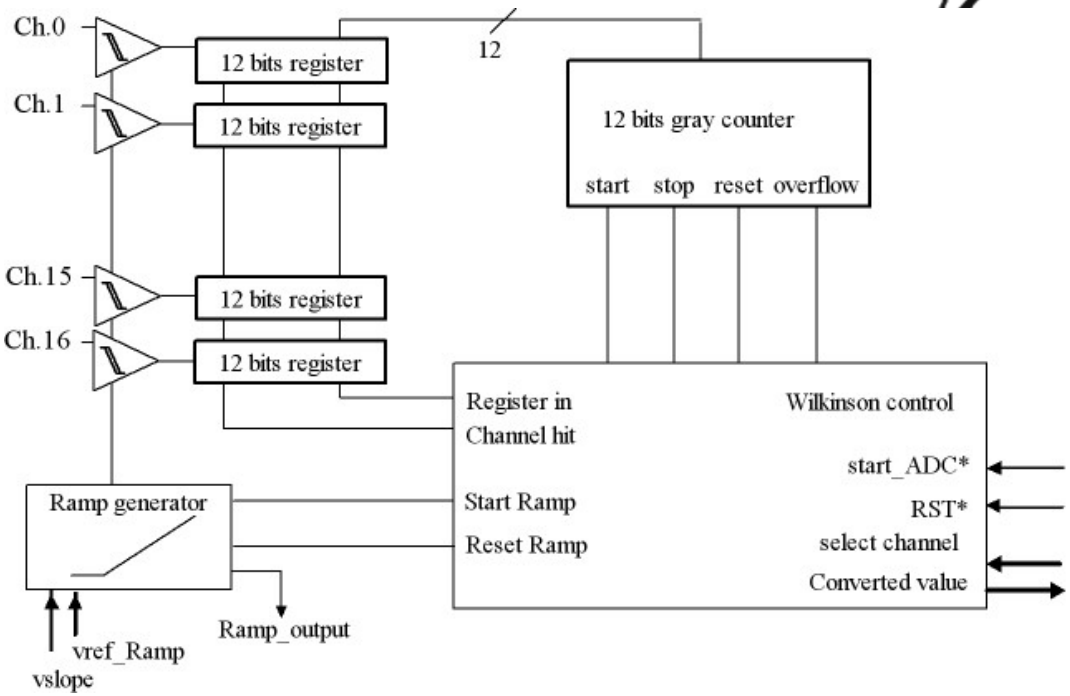


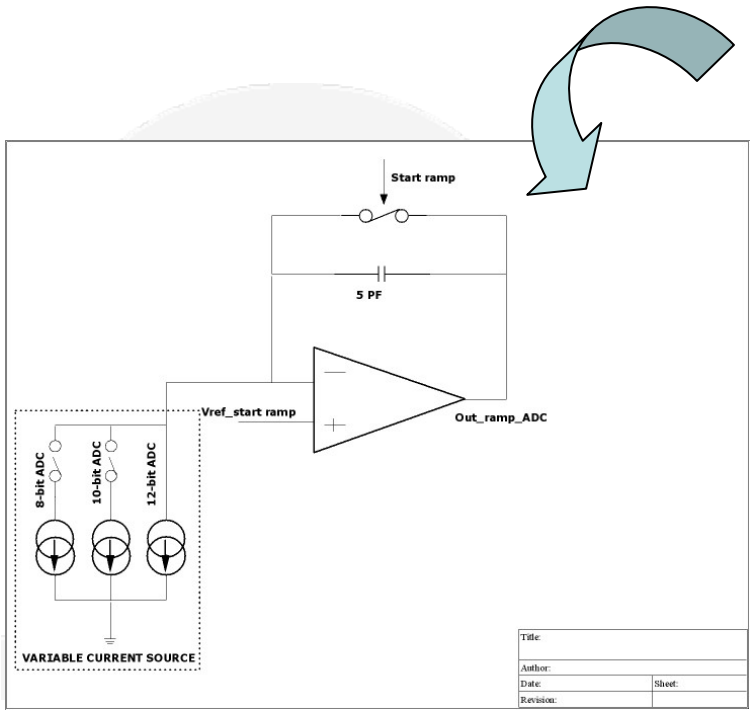
PARISROC architecture

Complete front-end chip with 16 independent auto trigger channels
Technology :Austria-Micro-Systems (AMS) SiGe 0.35 µm
Area:17 mm2 (5mm × 3.4mm)
Power Supply: 3.3V
Package: CQFP 160

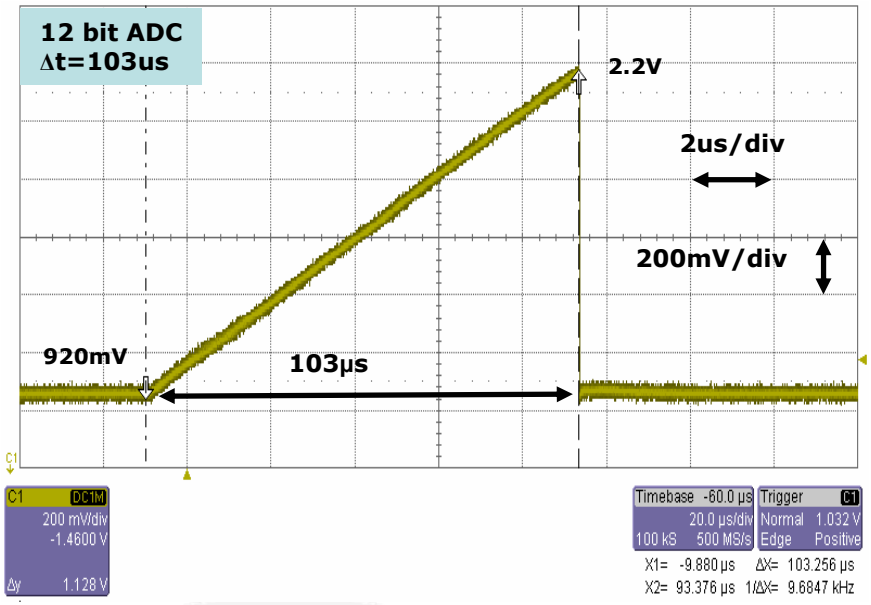


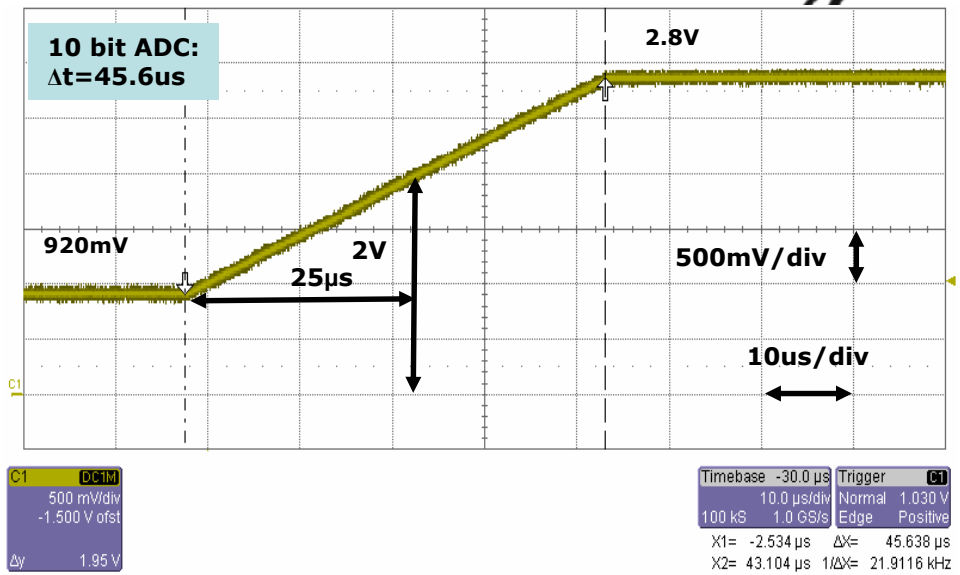
ADC schematics



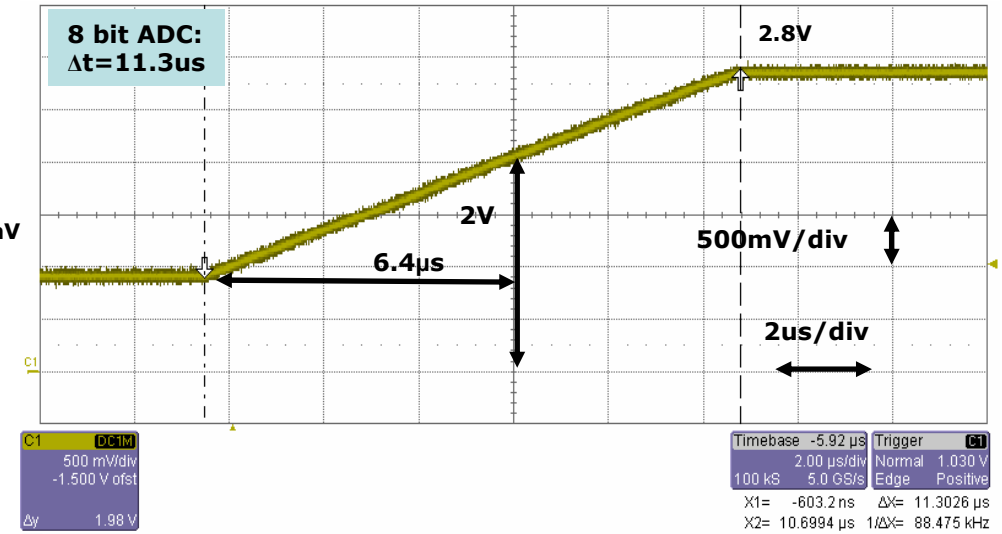


8/10/12-bit ADC RAMPS





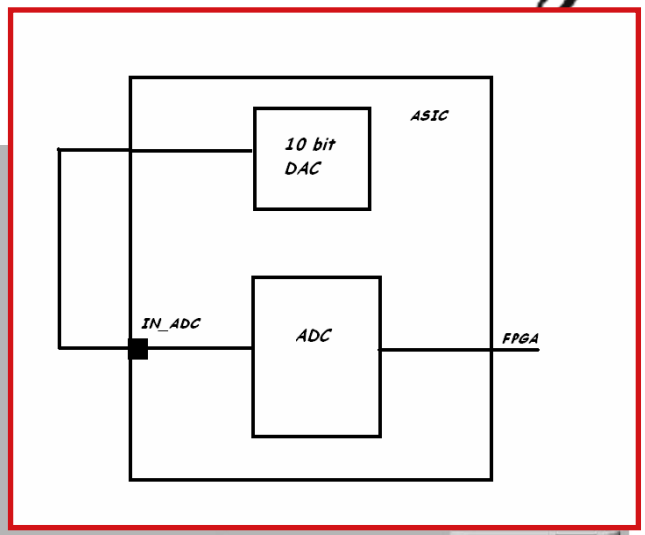
- **12-bit ADC:**
  2^{12}=4096*25ns (40MHz clock)=**102.4µs**
- **10-bit ADC:**
  2^{10}=1024*25ns (40MHz clock)=**25.6µs**
- **8-bit ADC:**
  2^{8}=256*25ns (40MHz clock)=**6.4µs**



ADC characterization

DAC=500=1.4523V
Number of acquisitions: 10000

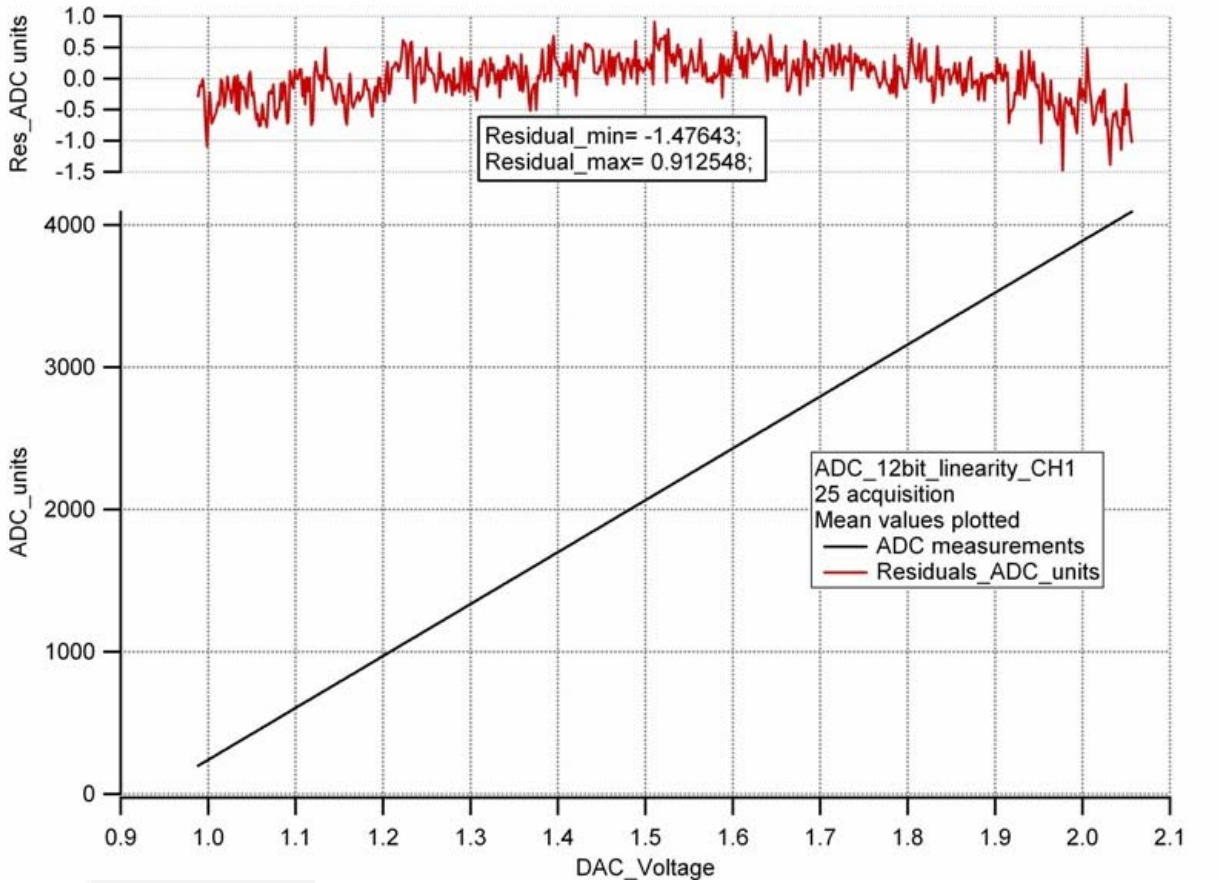
12 bit ADC (LSB=269µV)
ADC_UNITS=1961
ΔADC_units=5 (1.3mV)



12-bit ADC Linearity (INL)

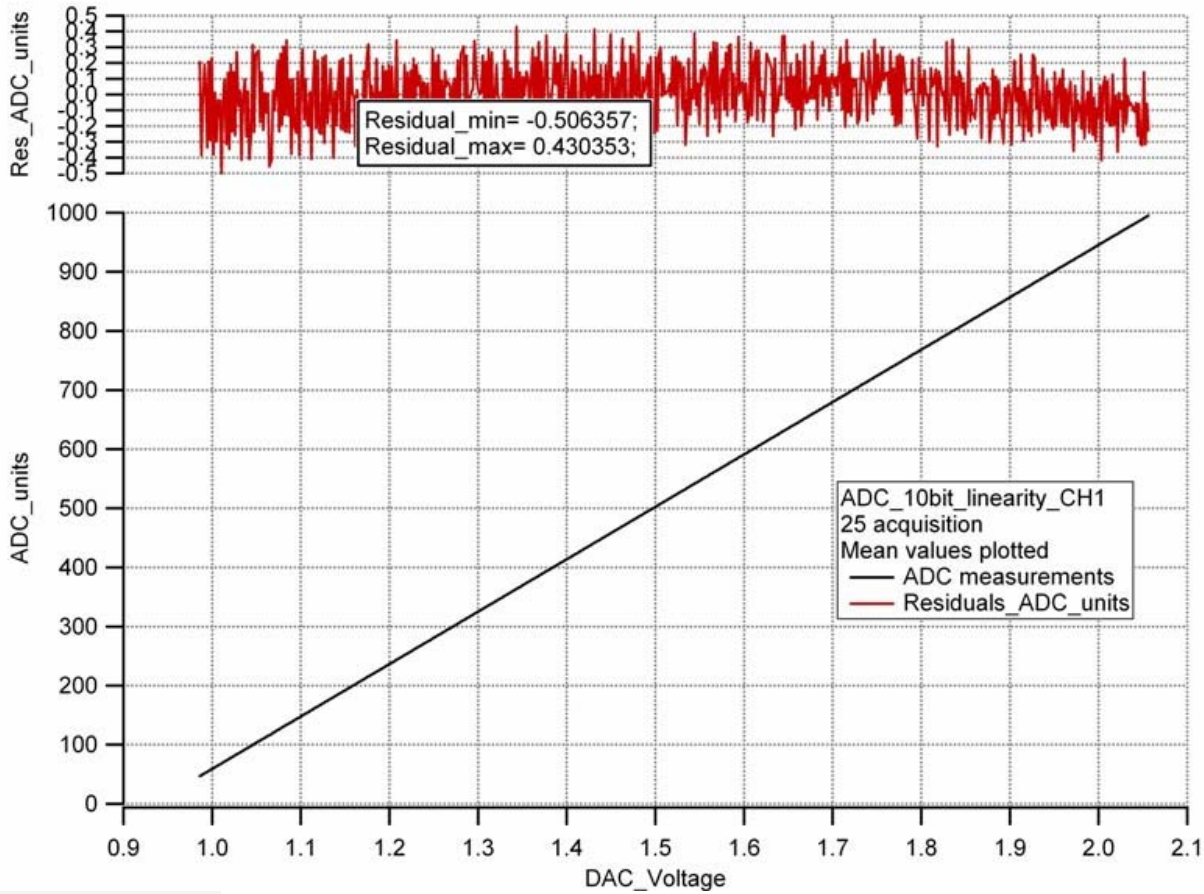
12 bit ADC
25 acquisitions
Vref_ramp ADC=0.968V
Vmax_ramp_ADC=2.07V
LSB=269uV
Residuals: from -1.5 to 0.9 (ADC units)

Mean values of 25 acquisitions are plotted!!!!



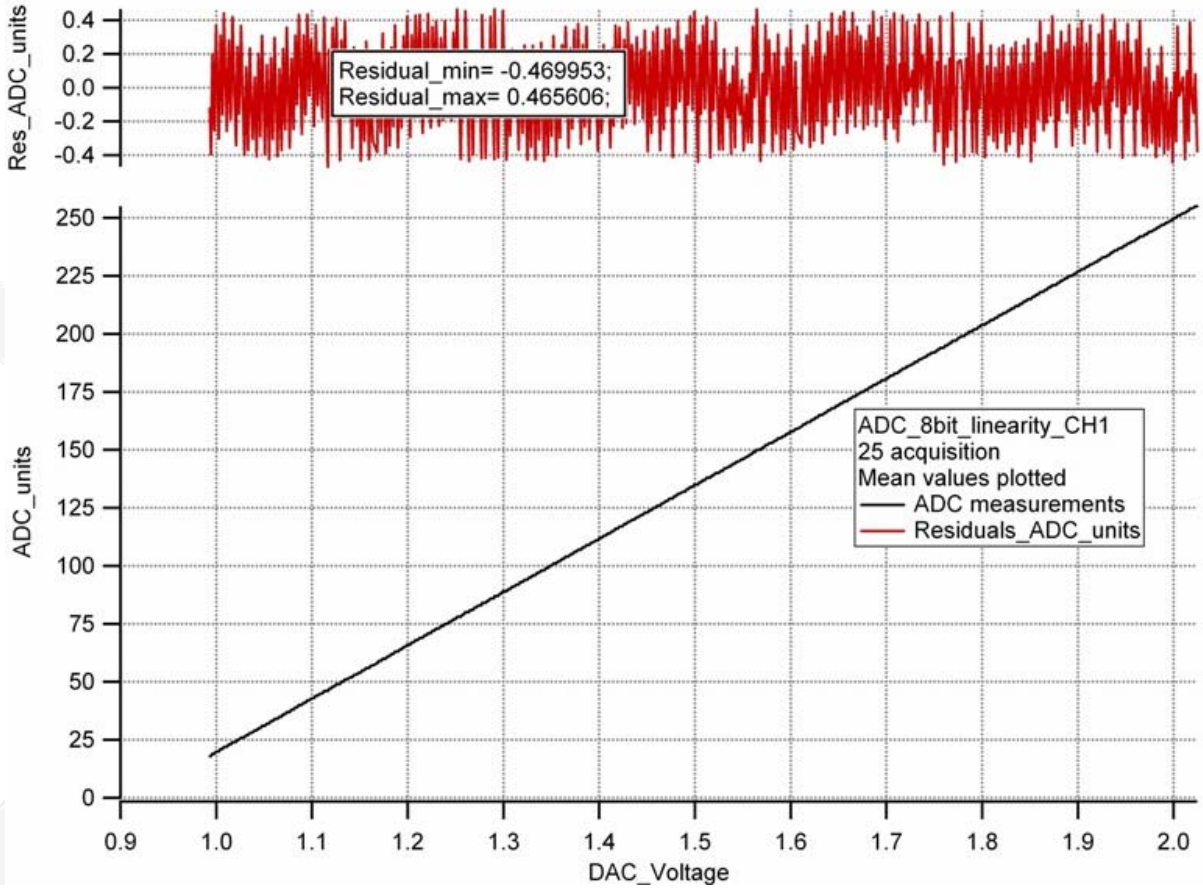
10-bit ADC Linearity (INL)

10 bit ADC
25 acquisition
Vref_ramp ADC=0.980V
Vmax_ramp_ADC=2.07V
LSB=1.06mV
Residuals: from -0.5 to 0.4 (ADC units)



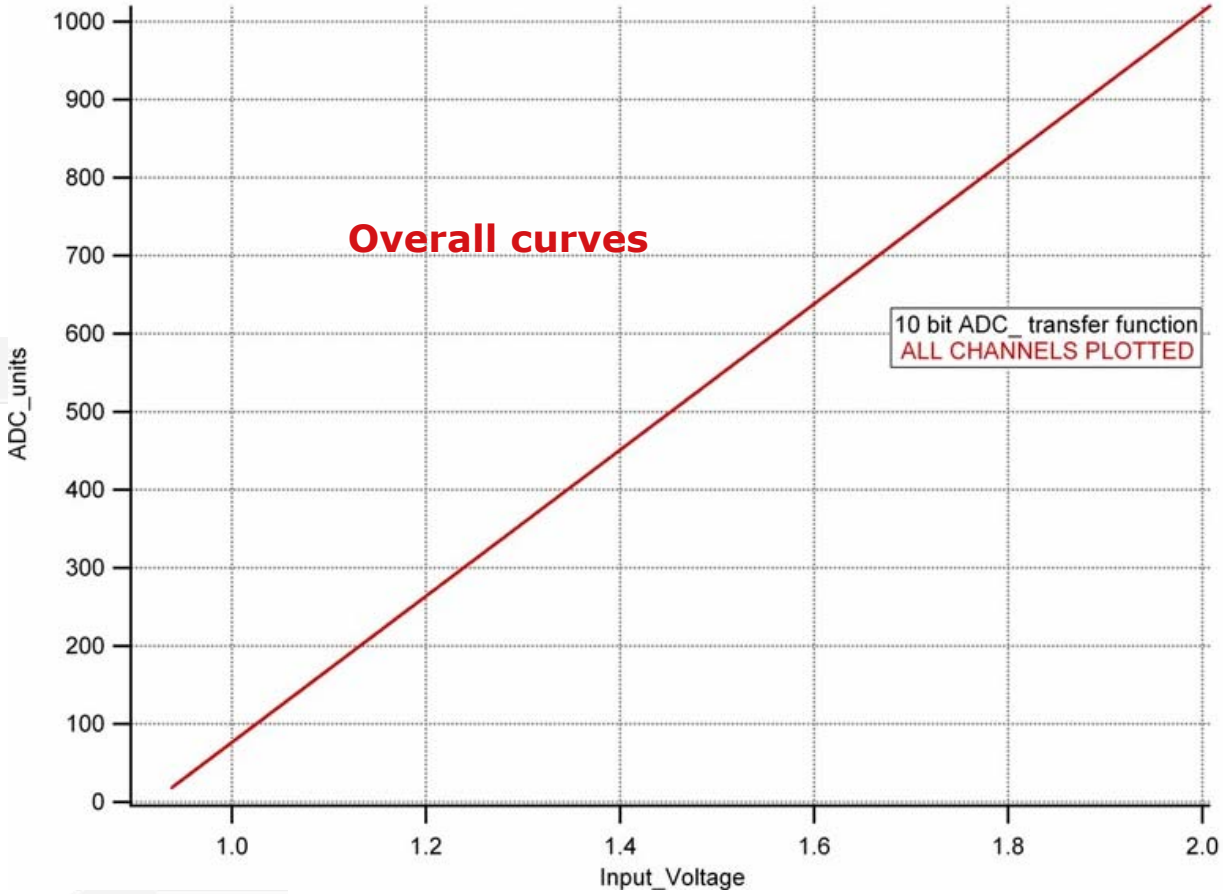
8-bit ADC Linearity (INL)

8 bit ADC
25 acquisition
Vref_ramp ADC=0.980V
Vmax_ramp_ADC=2.07V
LSB=4.26mV
Residuals: from -0.5 to 0.5



10bit-ADC Uniformity (I)

The ADC is suited to a multichannel conversion!!!!!

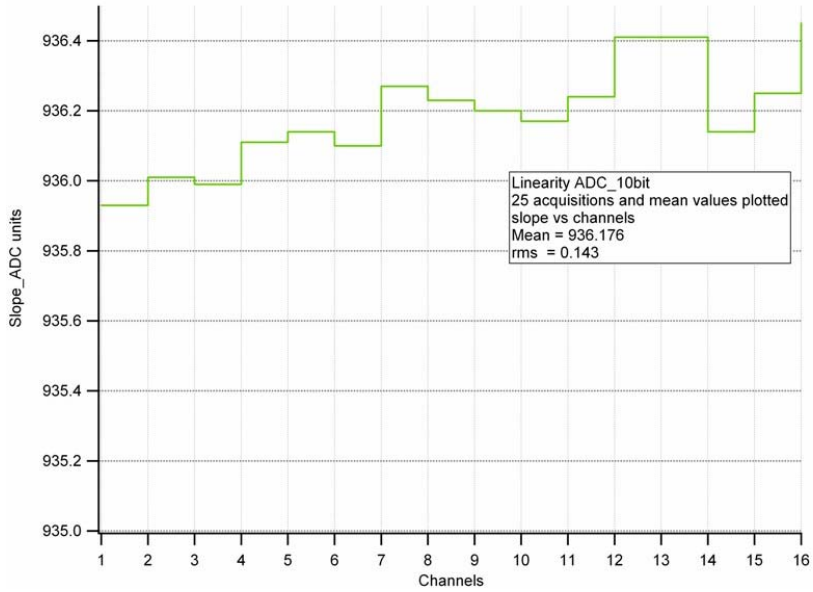


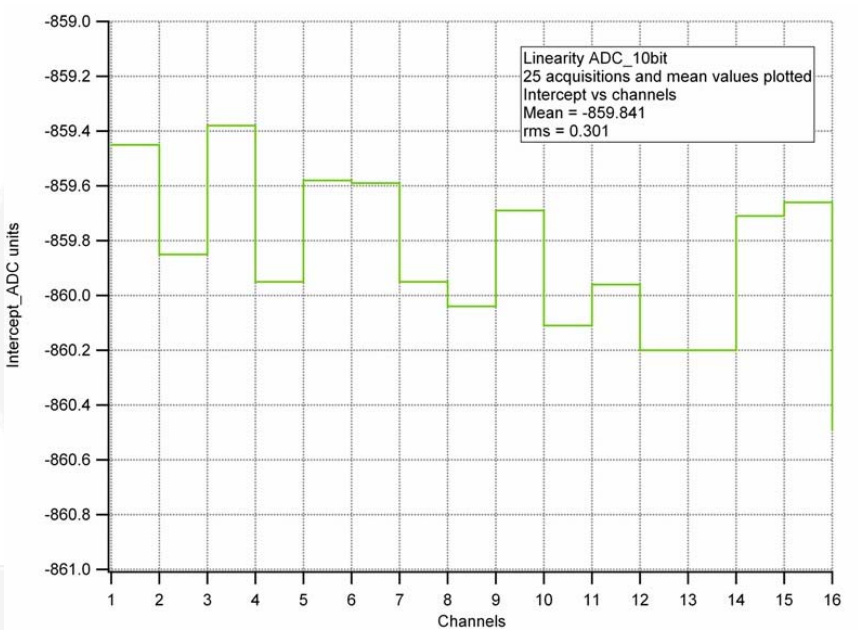
10 bit-ADC Uniformity (II)

Y(fit ADC)=mx+q Each channel
xmin=0.940mV (~vref_start_ramp) (DAC voltage input level)
ymin=21 UADC

Slope vs channels

10 bit ADC
25 acquisition
LSB=1.06mV
Mean=936.17
Rms=0.143=1*10^{-4}

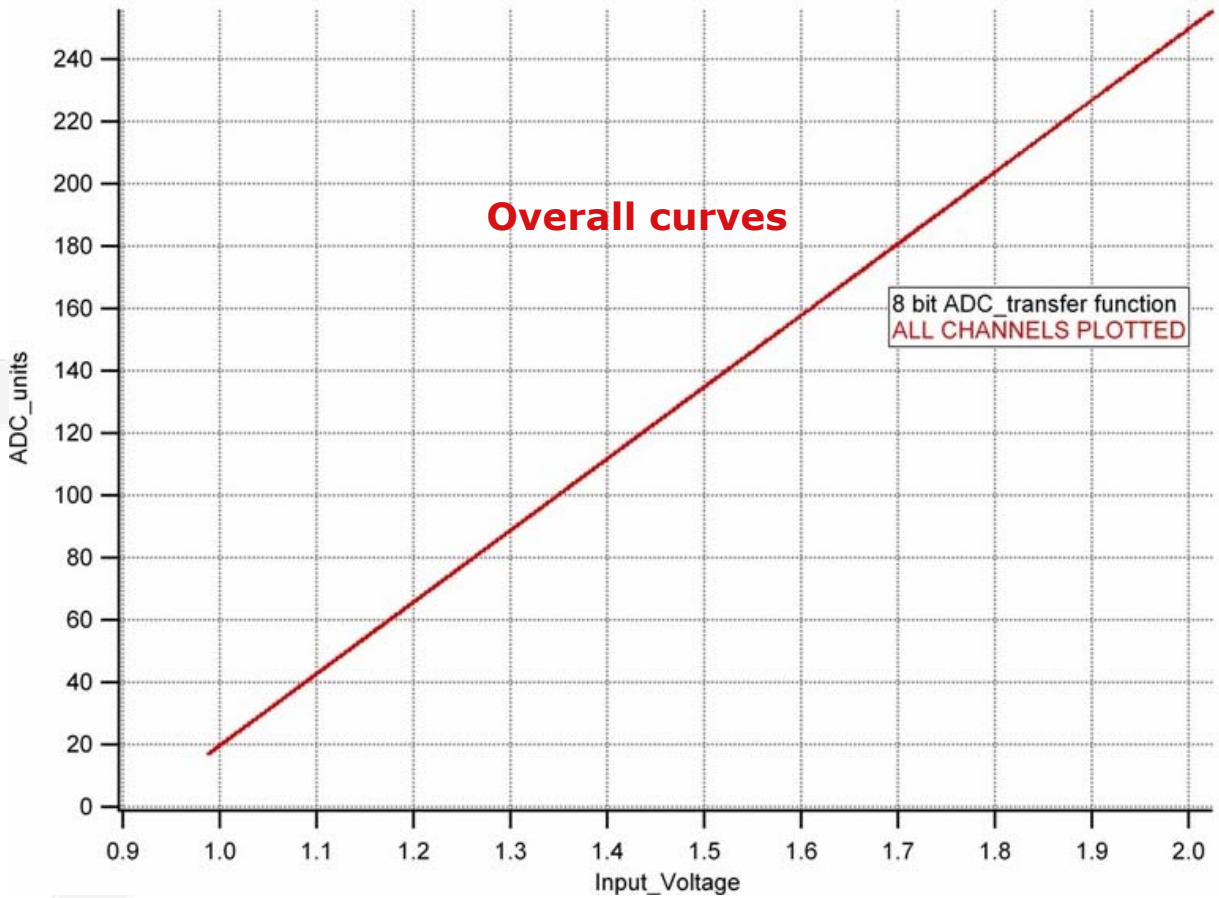




Intercept vs channels

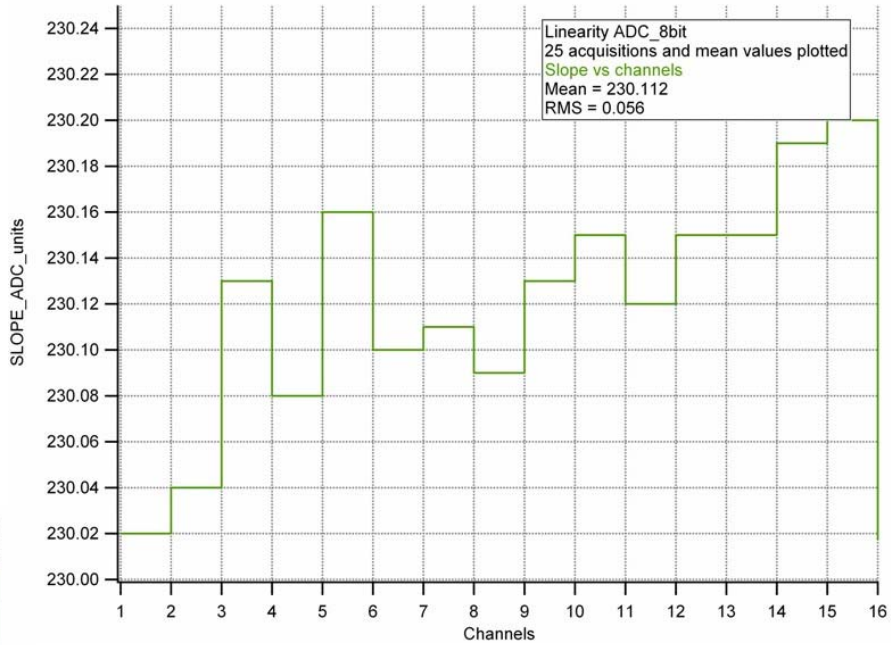
10 bit ADC:
25 acquisition
LSB=1.06mV
Mean=-859.841
Rms=0.301=1*10-4

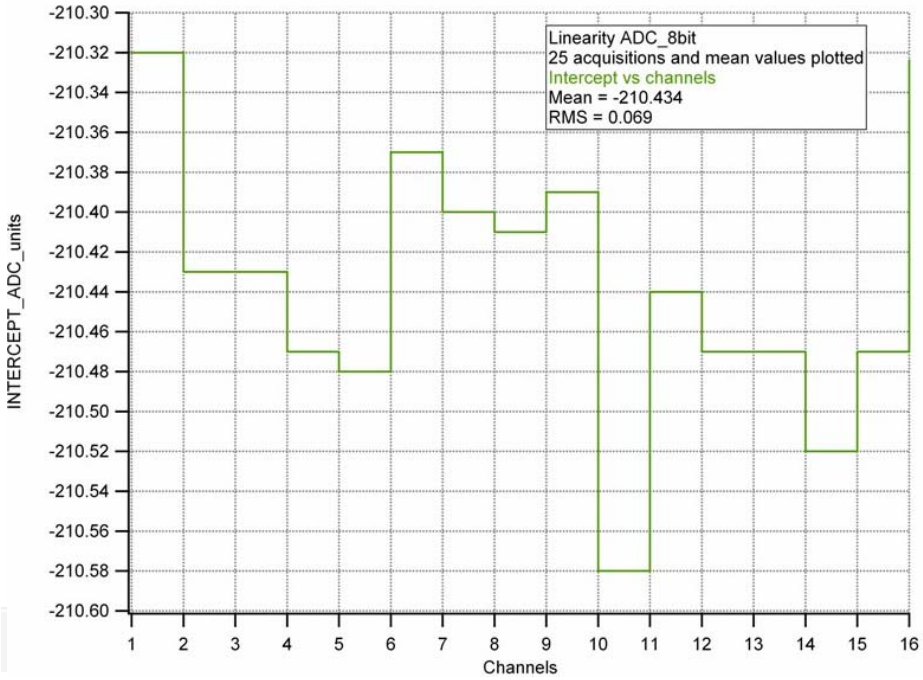
8 bit-ADC Uniformity (I)



8 bit-ADC Uniformity (II)

Slope vs channels
8 bit ADC:
25 acquisition
LSB=4.26mV
Mean=230
Rms=0.056=2*10-4

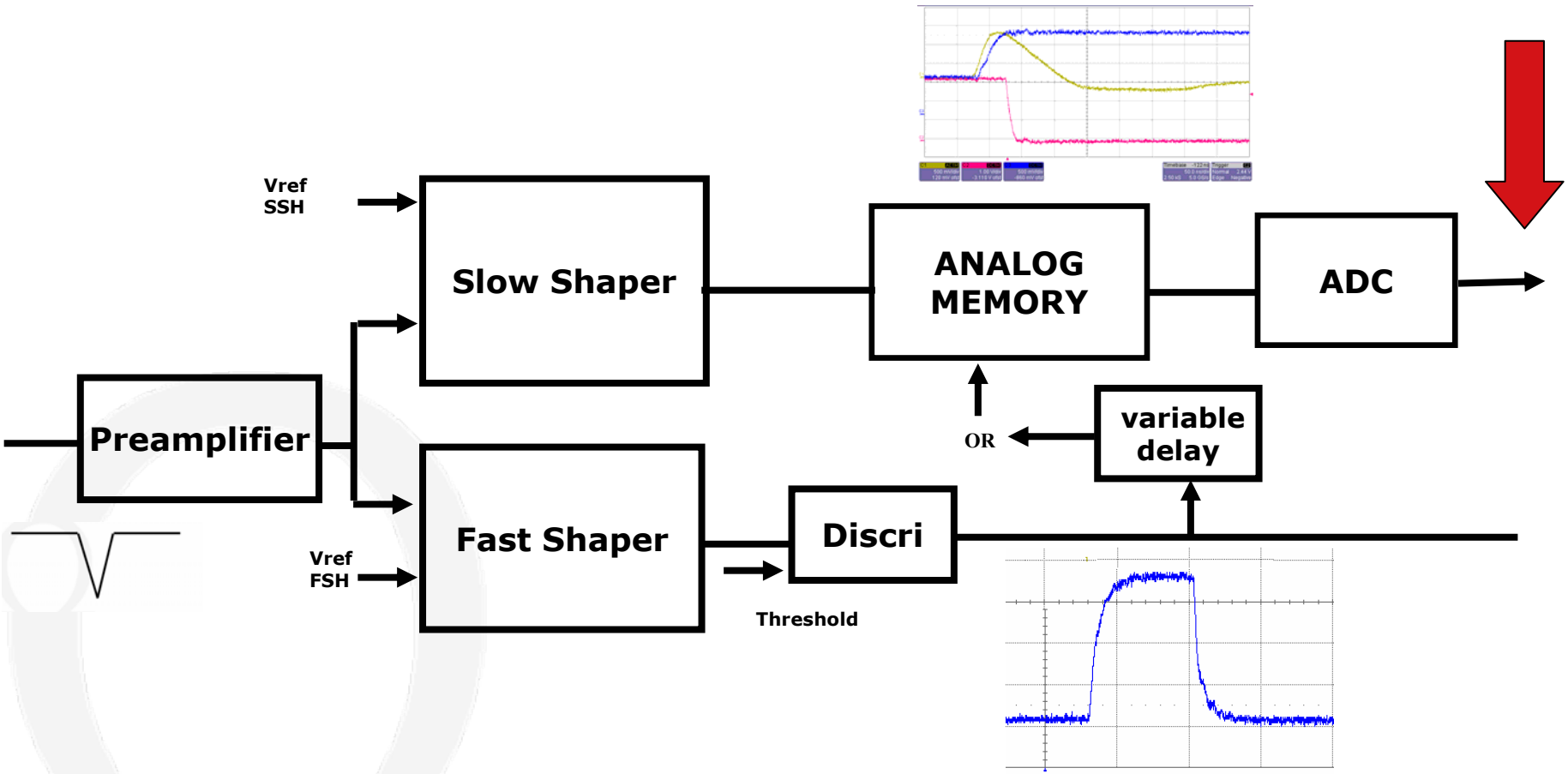




Intercept vs channels
8 bit ADC:
25 acquisition
LSB=4.26mV
Mean=-210
Rms=0.069=3*10-4

Overall behavior

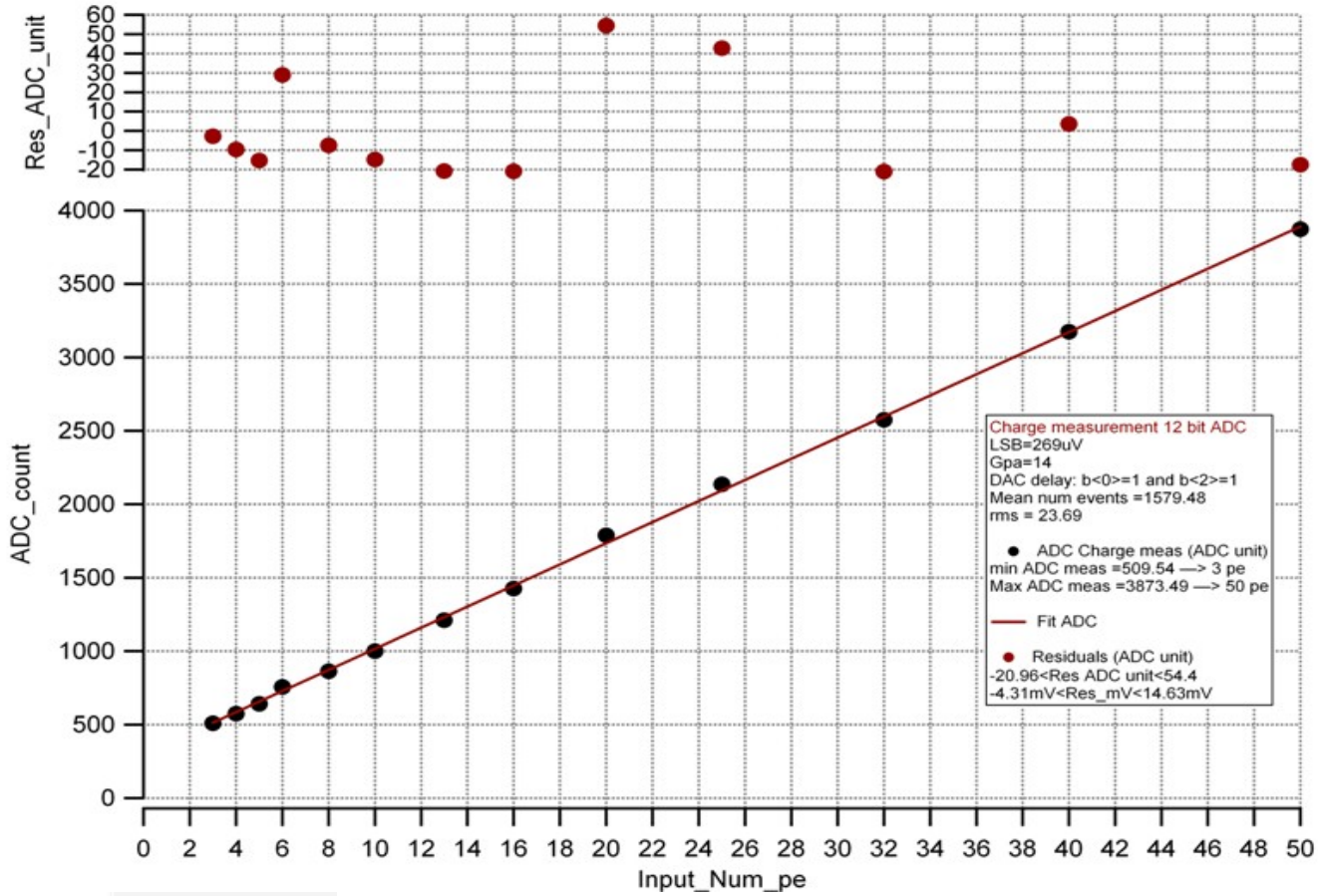
Complete chain: Autotrigger + T&H + Internal ADC



Overall behavior (12-bit ADC)

Linearity : 1% ; Noise 23 UADC (12 bit 269uV)

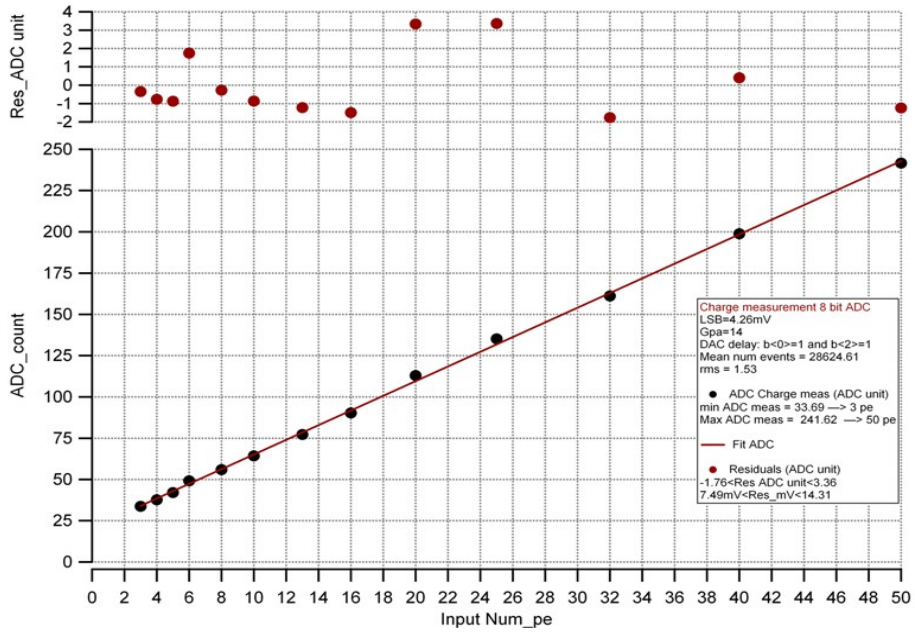
G_pa=14 (Cin=7pF , Cf=0.5pF)
Slow shaper=50ns

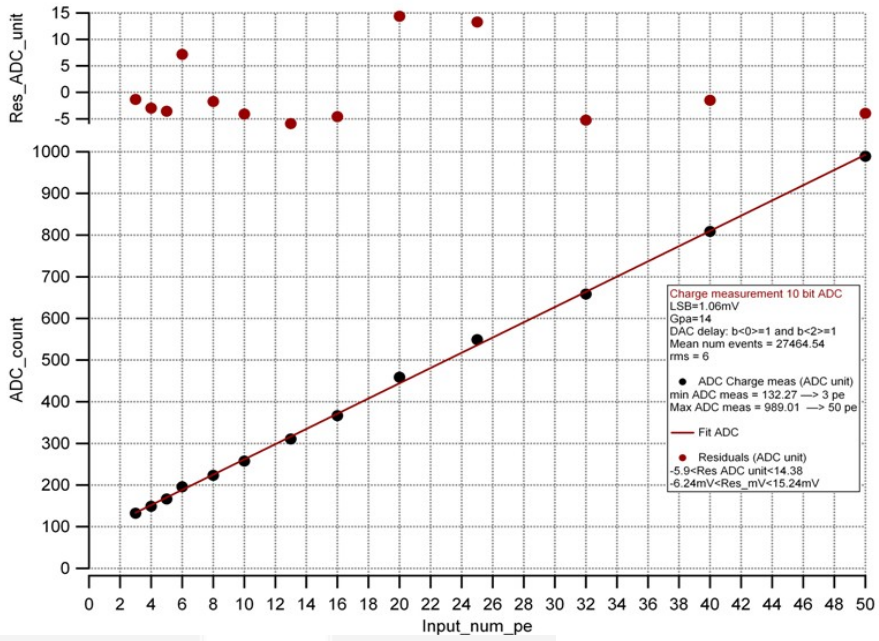


Overall behavior (10/8-bit ADC)

G_pa=14 (Cin=7pF , Cf=0.5pF)
Slow shaper=50ns

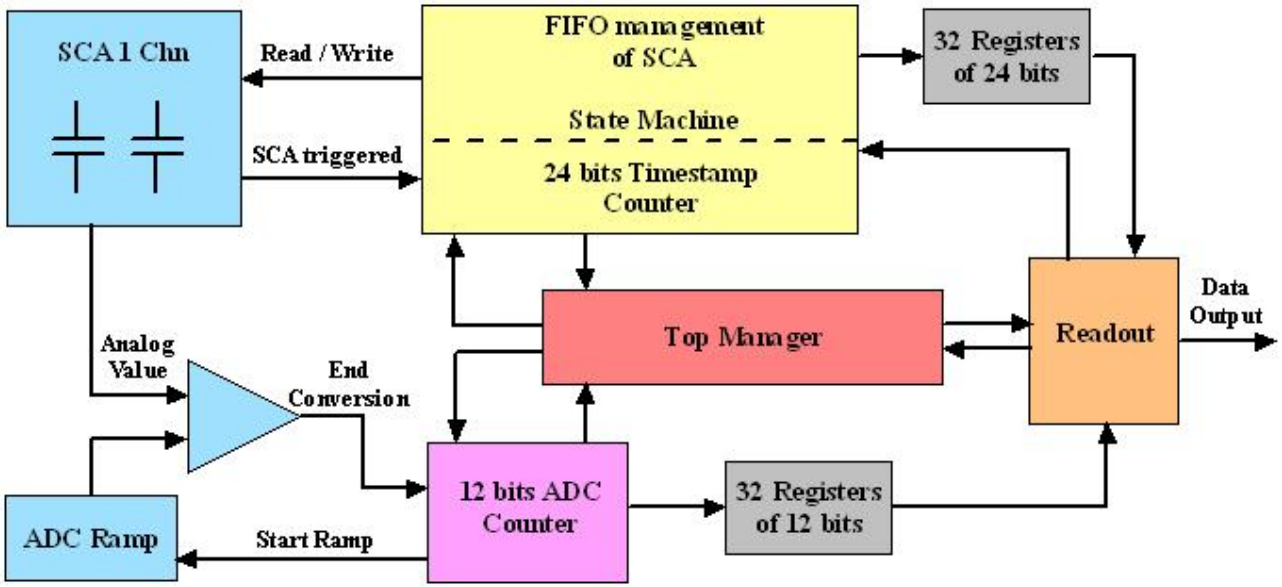
10-bit
Linearity : 1% ;
Noise 6 UADC (10-bit LSB=1.06mV)
8-bit
Linearity : 1% ;
Noise 1.5 UADC (8-bit LSB=4.26mV)





Backup slides

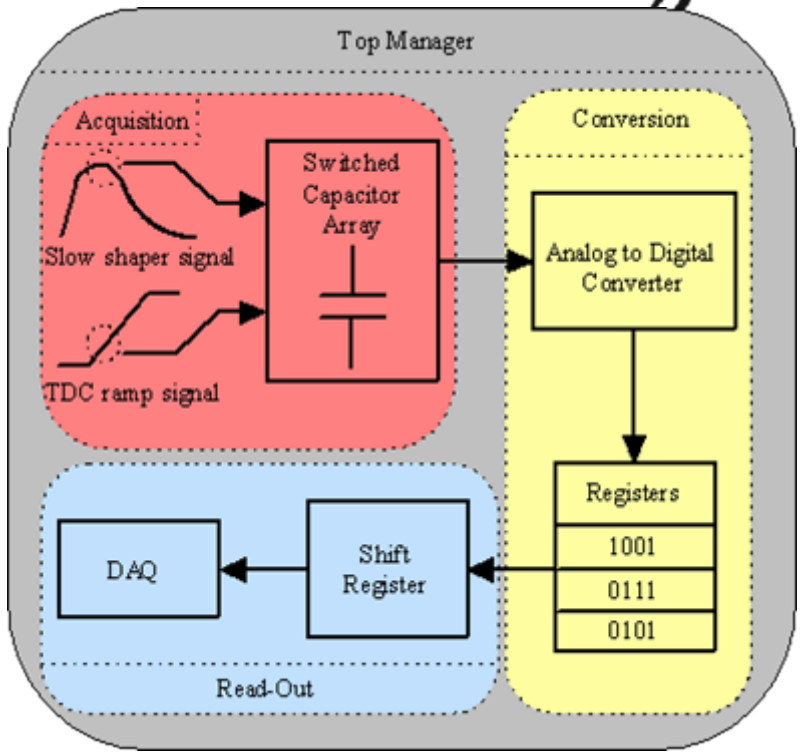
Digital part architecture(I)



- 16 channels managed independently
- 2 state machine dedicated to handle one channel: Write and Read
- SCA depth of 2 for time and charge measurement
- SCA management like FIFO
- 24bits Timestamp counter @ 10 MHz (1.67s)
- 32 registers of 24 bits to save coarse time for each depth of SCA
- 32 registers of 12 bits to store converted data: 16 charge and 16 fine time
- 40 MHz clock for ADC + SCA management
- 10 MHz clock for Timestamp + Readout

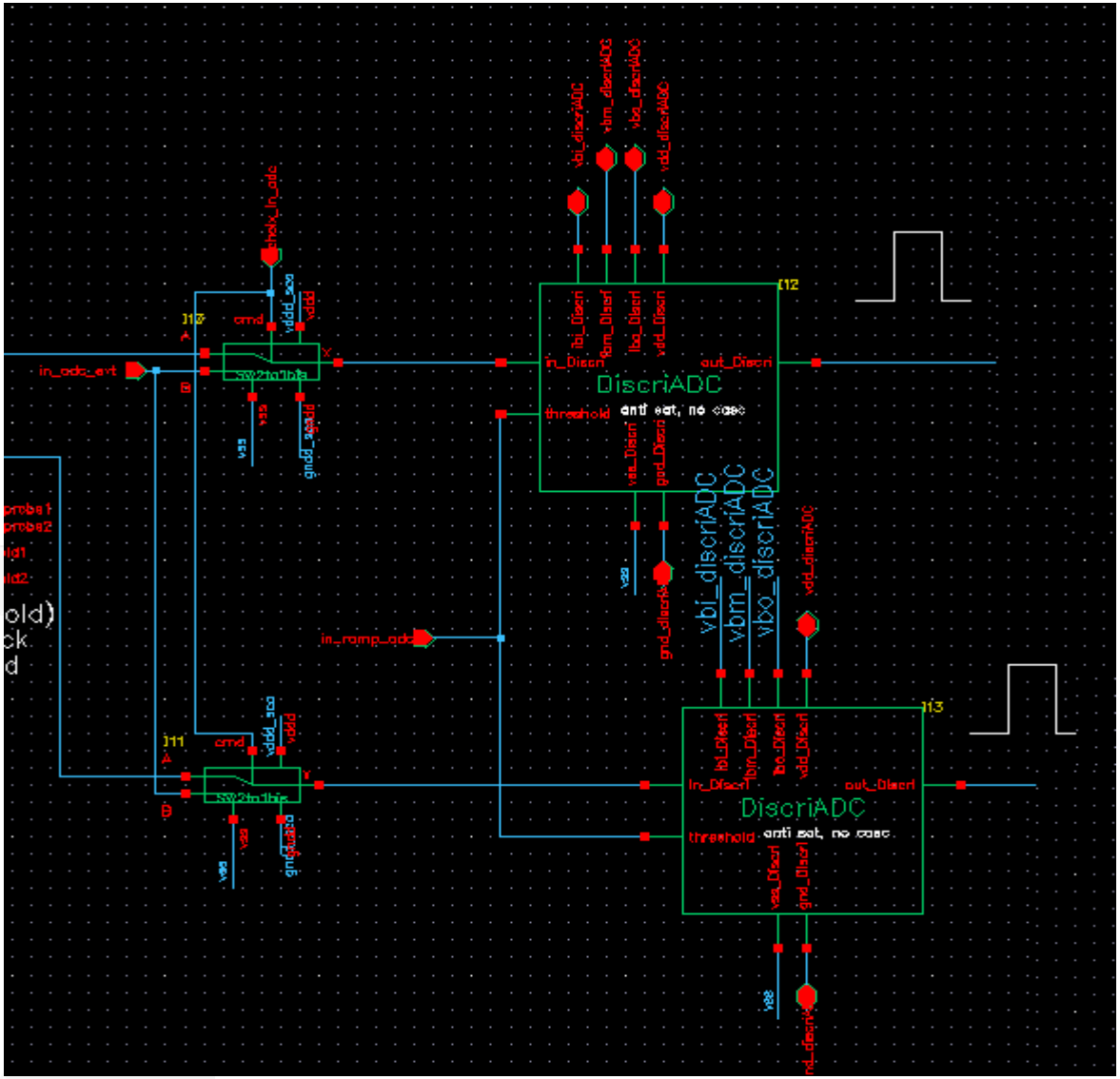
Digital part architecture(II)

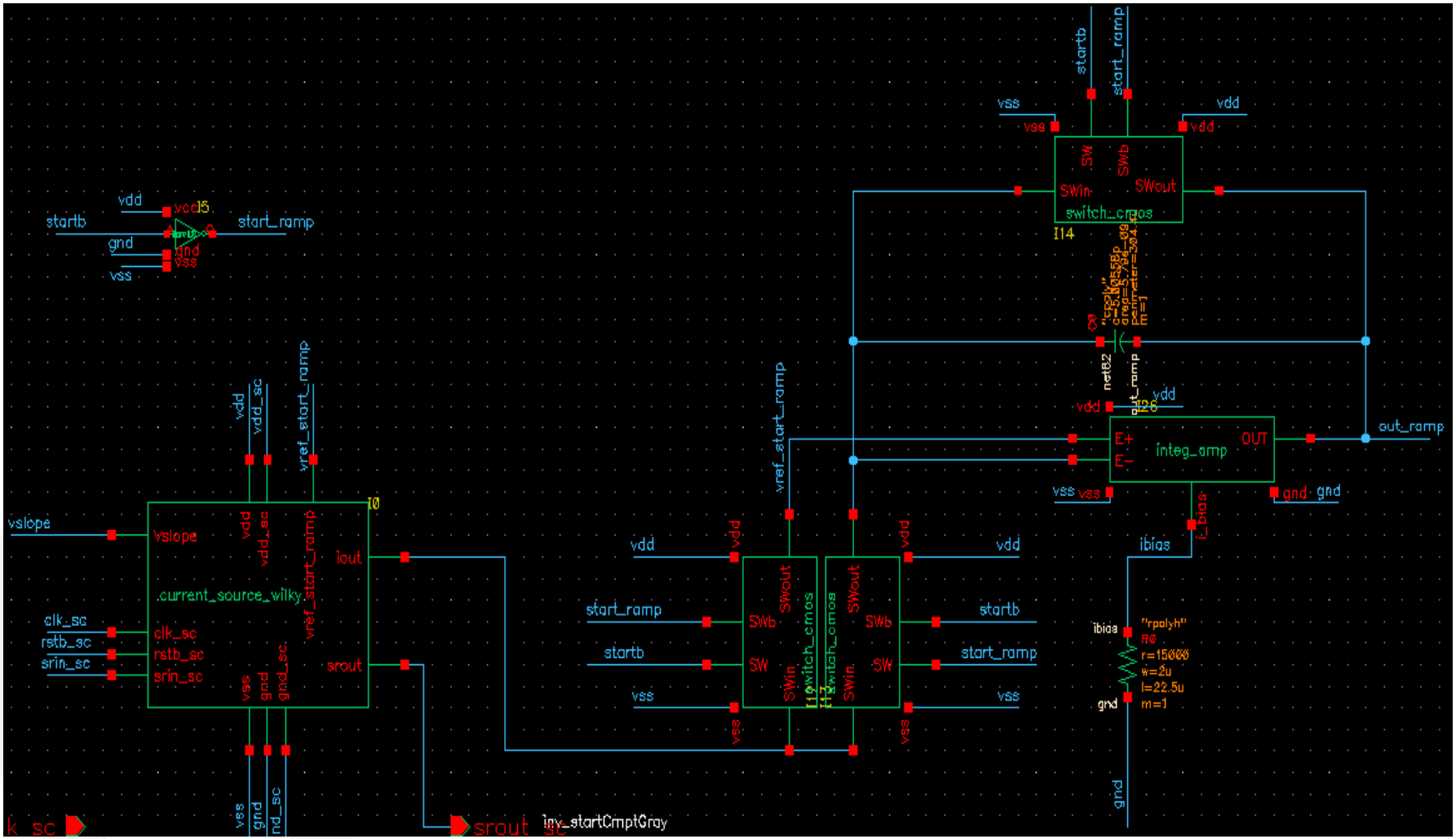
- 4 modules: *Acquisition, Conversion, Read Out and Top manager.*
- Acquisition: Analog memory
- Conversion: Analog charge and time into 12 bits digital value saved in register (RAM)
- Read Out: RAM read out to an external system

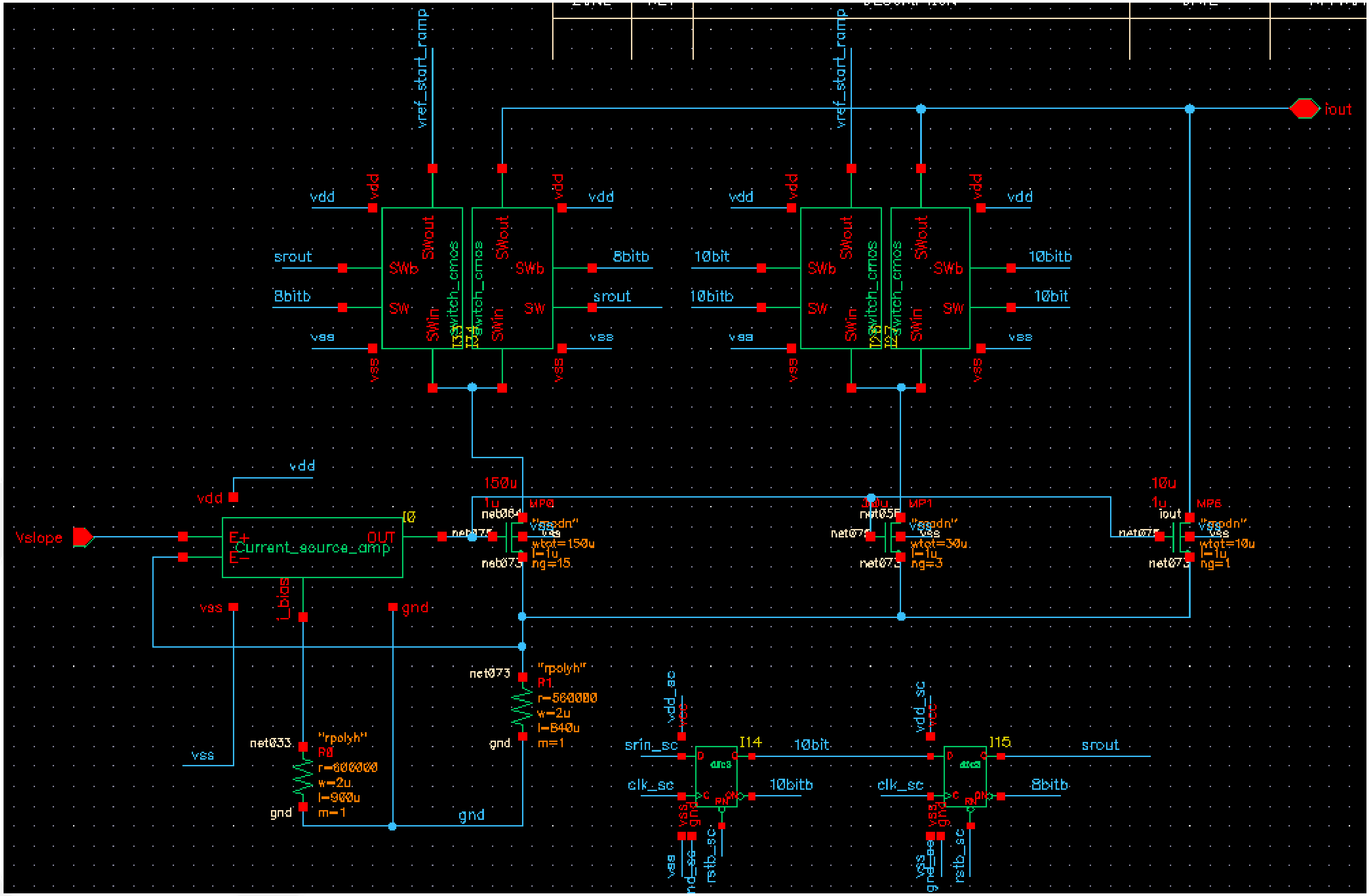


Selective Read Out

- Only hit channels are readout
- Readout clock : 10 MHz
- Max Readout time (16 ch hit) : 100 us
- 52 bits of data / hit channel (all gray)
- Readout format (MSB first) : 4 bits channel # +
  24 bits timestamp +
  12 bits charge +
  12 bits time


DiscriADC
anti eat, no coec
threshold
in_ramp_adc
vbi_discriADC
vbm_discriADC
vbo_discriADC
out_Discri


startb
start_ramp
vss
vdd
SW
SWb
SWin
SWout
switch_cmos
I14
vdd
vcdl5
gnd
vss
vdd_sc
vref_start_ramp
I0
vslope
.current_source_wilky
iout
clk_sc
rstb_sc
srin_sc
srout
gnd_sc
out_ramp
E+
E-
integ_amp
OUT
ibias
i_bias
"rpolyh"
R0
r=15000
w=2u
l=22.5u
m=1
srout
startCmptGray


vref_start_ramp
iout
vdd
srout
8bitb
vss
SWb
SW
SWout
SWin
switch_cmos
10bit
10bitb
vslope
E+
E-
Current_source_amp
OUT
I0
i_bias
gnd
MP0
MP1
MP6
"rpolyh"
R1
r=560000
w=2u
l=840u
m=1
R0
r=600000
l=900u
net073
net033
I14
I15
srin_sc
clk_sc
rstb_sc
vdd_sc